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**AG6200-MDQ**

**HDMI to VGA Converter**

**Data Sheet V1.4**

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## Change History

Version	Date	Notes
1.0	2016.3	First Released
1.1	2017.4	Update package size
1.2	2018.1	Revise ASIC P/N from AG6200B to AG6200-MCQ
1.3	2019.1	Modify Table 2 Normal Operating Conditions
1.4	2019.4	Revise ASIC P/N from AG6200-MCQ to AG6200-MDQ

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### Features

- Convert HDMI 1.4b to VGA
- Video resolution support up to 1920x1200@60Hz:
- Support hot plug detect
- Embedded Crystal, Crystal-less in components.
- Embedded Regulator of 5V to 1.2V
- Core power 1.2 V
- On-chip HDCP Engine which is compliant with HDCP 1.4 specification
- Integrated on-chip HDCP Keys
- Support 2 channel IIS audio interface
- Support 1080i resolution

### Packaging

- Package size: 48-pin QFN, 6 mm x 6 mm
- Extended commercial temperature range (0°C to +85°C)

### Applications

- Cable adaptors
- Docking Stations

### General Description

The Algotek AG6200-MDQ chip is a HDMI (High Definition Multimedia Interface) to VGA bridge IC. It converts HDMI signal to standard VGA signal. It can be designed in devices such as adapters, smart cables.

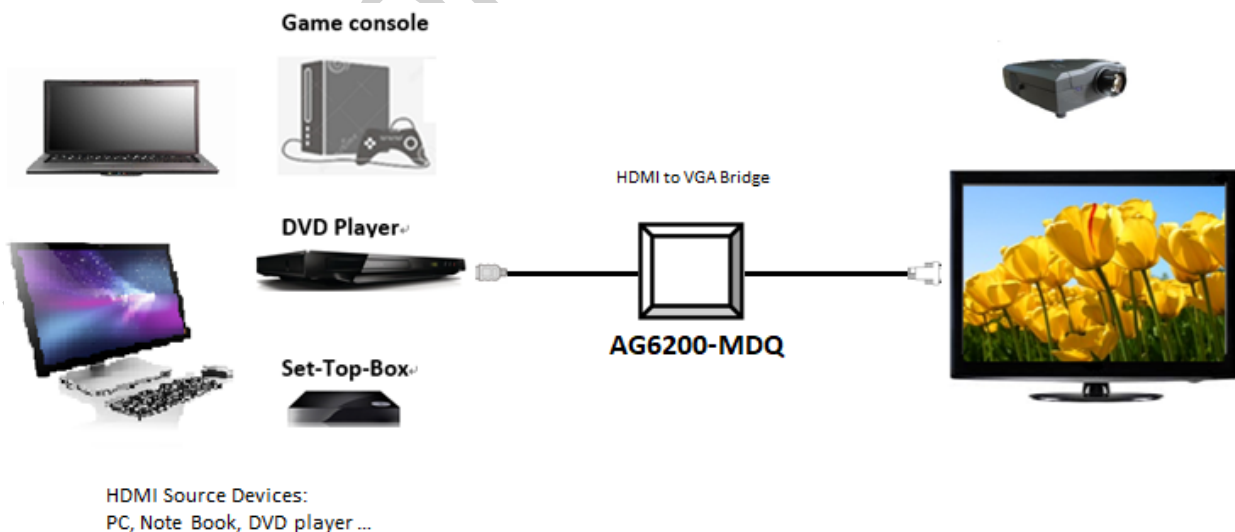


Figure 1 Application for HDMI to VGA Bridge

# 1. System Block and Functional Description

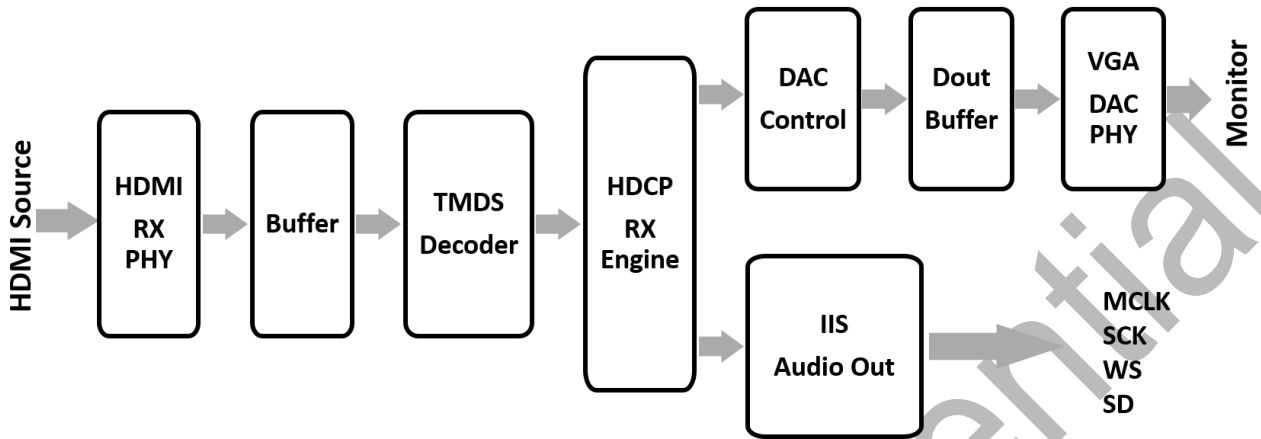


Figure 2 System Block Diagram

## Pin Mapping

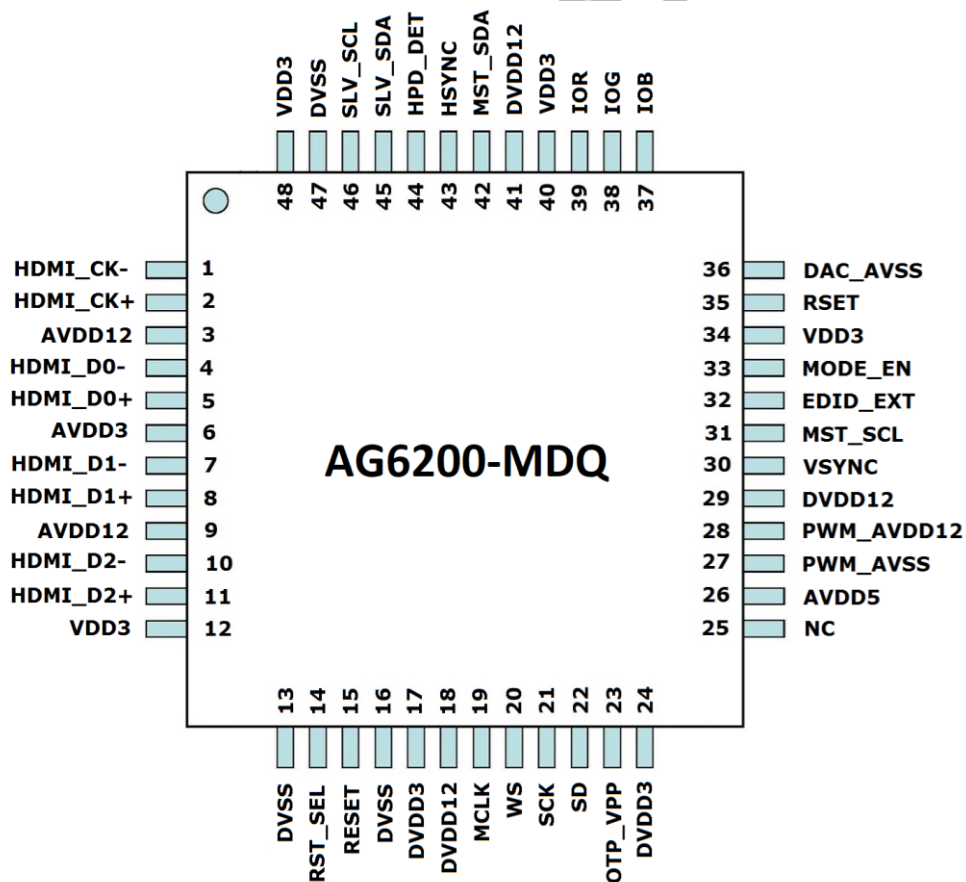


Figure 3 48-Pin Mapping

## Pin Description

PIN NO.	Package Pin Name	Type	Description
1	HDMI_CK-	Input	HDMI Receiver clock negative input
2	HDMI_CK+	Input	HDMI Receiver clock positive input
3	AVDD12	Power	HDMI 1.2V power
4	HDMI_D0-	Input	HDMI Receiver channel-0 negative input
5	HDMI_D0+	Input	HDMI Receiver channel-0 positive input
6	AVDD3	Power	HDMI 3.3V power
7	HDMI_D1-	Input	HDMI Receiver channel-1 negative input
8	HDMI_D1+	Input	HDMI Receiver channel-1 positive input
9	AVDD12	Power	HDMI 1.2V power
10	HDMI_D2-	Input	HDMI Receiver channel-2 negative input
11	HDMI_D2+	Input	HDMI Receiver channel-2 positive input
12	VDD3	Power	HDMI 3.3V power
13	DVSS	Power	Ground
14	RST_SEL	Input	POR or input reset select
15	RESET	Input	Reset Input
16	DVSS	Power	Ground
17	DVDD3	Power	Digital 3.3V power
18	DVDD12	Power	Digital 1.2V power
19	MCLK	Output	I2S System Clock
20	WS	Output	I2S Word Select
21	SCK	Output	I2S Continuous Serial Clock
22	SD	Output	I2S Serial Data Output
23	OTP_VPP	Power	OTP 3.3V/6.5V power
24	DVDD3	Power	Digital 3.3V power
25	N.C	N.C	N.C
26	AVDD5	Power	PWM & LDO 5V input
27	PWM_AVSS	Power	Ground
28	PWM_AVDD12	Power	PWM 1.2V output
29	DVDD12	Power	Digital 1.2V power
30	VSYNC	Output	V_SYNC
31	MST_SCL	Bidirectional	VGA I2C SCL
32	EDID_EXT	Input	EDID Extension bit

PIN NO.	Package Pin Name	Type	Description
33	MODE_EN	Input	Reserve
34	VDD3	Power	DAC analog & Digital 3.3V power
35	RSET	Input	output 4.7k $\Omega$ to GND
36	DAC_AVSS	Power	DAC Ground
37	IOB	Output	Blue output 75 $\Omega$ to GND
38	IOG	Output	Green output 75 $\Omega$ to GND
39	IOR	Output	Red output 75 $\Omega$ to GND
40	VDD3	Power	DAC analog & Digital 3.3V power
41	DVDD12	Power	Digital 1.2V power
42	MST_SDA	Bidirectional	VGA I2C SDA
43	HSYNC	Output	H_SYNC
44	HPD_DET	Bidirectional	HDMI Hot Plug
45	SLV_SDA	Bidirectional	HDMI Display Data Channel (DDC) SDA
46	SLV_SCL	Bidirectional	HDMI Display Data Channel (DDC) SCL
47	DVSS	Power	Ground
48	VDD3	Power	Digital & HDMI 3.3V power

**Table 1 Pin Description**

## 2. Electrical Characteristics

### Normal Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
AVDD12, DVDD12, PWM_AVDD12	1.2V Power	1.08	1.2	1.32	V
AVDD3, VDD3, DVDD3	3.3V Power	3.0	3.3	3.6	V
AVDD5	5V Power Input for LDO 5V-to-3.3V	4.5	5	5.5	V
OTP_VPP	3.3V Power for read	3.0	3.3	3.6	V
	6.5V Power for write	6.3	6.5	6.7	V
$\theta_{JC}$	Thermal Resistance (Junction to Case)		2		$^{\circ}\text{C}/\text{W}$
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)		33		$^{\circ}\text{C}/\text{W}$
TJ	Junction Temperature	0	25	125	$^{\circ}\text{C}$
Ta	Ambient Temperature	0	25	85	$^{\circ}\text{C}$

**Table 2 Normal Operating Conditions**



## DC Specification

Symbol	Parameter	Frequency	VDD	AVDD PLL <sup>2</sup>	AVDD	VDDH	VDD5V _IN	VDDIO	XTALV CC33	Units
			1.2V	1.2V	1.2V	3.3 V	5.0 V	3.3 V	3.3 V	
I <sub>DDSB</sub>	No input current	—	7.20	—	18.35	—	5.90	<1	—	mA

**Table 3 DC Power Typical Supply Specifications**

Symbol	Parameter	Frequency	VDD	AVDD PLL <sup>2</sup>	AVDD	VDDH	VDD5V _IN	VDDIO	XTALV CC33	Units
			1.2V	1.2V	1.2V	3.3 V	5.0 V	3.3 V	3.3 V	
I <sub>DDSB</sub>	No input current	—	80	—	40	—	6	<1	—	mA

**Table 4 DC Power Maximum Supply Specifications**

Symbol	Parameter	Pin Type	Conditions	Min	Typ.	Max	Units
V <sub>TH+DDC</sub>	LOW to HIGH threshold, DDC interface	Schmitt	—	2.0	—	—	V
V <sub>TH-DDC</sub>	HIGH to LOW threshold DDC interface	Schmitt	—	—	—	0.8	V
V <sub>TH+CEC_A</sub>	LOW to HIGH threshold, CEC_A pin	Schmitt	—	2.0	—	—	V
V <sub>TH-CEC_A</sub>	HIGH to LOW threshold, CEC_A pin	Schmitt	—	—	—	0.8	V
V <sub>TH+I2C</sub>	LOW-to-HIGH Threshold, I <sup>2</sup> C Bus	Schmitt	—	2.0	—	—	V
V <sub>TH-I2C</sub>	HIGH-to-LOW Threshold, I <sup>2</sup> C Bus	Schmitt	—	—	—	0.8	V
V <sub>TH+</sub>	LOW to HIGH threshold	LVTTTL Schmitt	—	2.0	—	—	V
V <sub>TH-</sub>	HIGH to LOW threshold	LVTTTL Schmitt	—	—	—	0.8	V
V <sub>OL_DDC</sub>	LOW-level Output Voltage, DDC interface	Open Drain	I <sub>OL</sub> = -3 mA	—	—	0.4	V
V <sub>OL_I2C</sub>	LOW-level Output Voltage I <sup>2</sup> C Bus	Open Drain	I <sub>OL</sub> = -3 mA	—	—	0.4	V
I <sub>Oz</sub>	Output leakage current	—	High impedance	—	—	±1	μA
I <sub>IL</sub>	Input leakage current	—	—	—	—	±1	μA
I <sub>OD</sub>	General digital output drive	LVTTTL/Output	V <sub>OH</sub> = 2.4 V	7.5	—	—	mA
			V <sub>OL</sub> = 0.4 V		—	—	mA
I <sub>ODCEC_A</sub>	CEC_A digital output drive	Schmitt	V <sub>OH</sub> = 2.4 V	4.0	—	—	mA
			V <sub>OL</sub> = 0.4 V		—	—	mA

**Table 5 Digital I/O Specification**

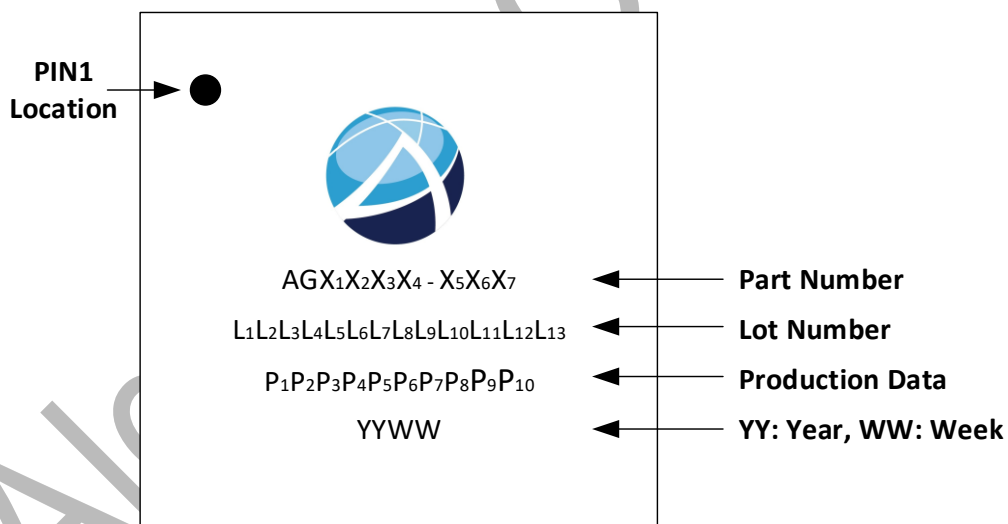
## AC Specification

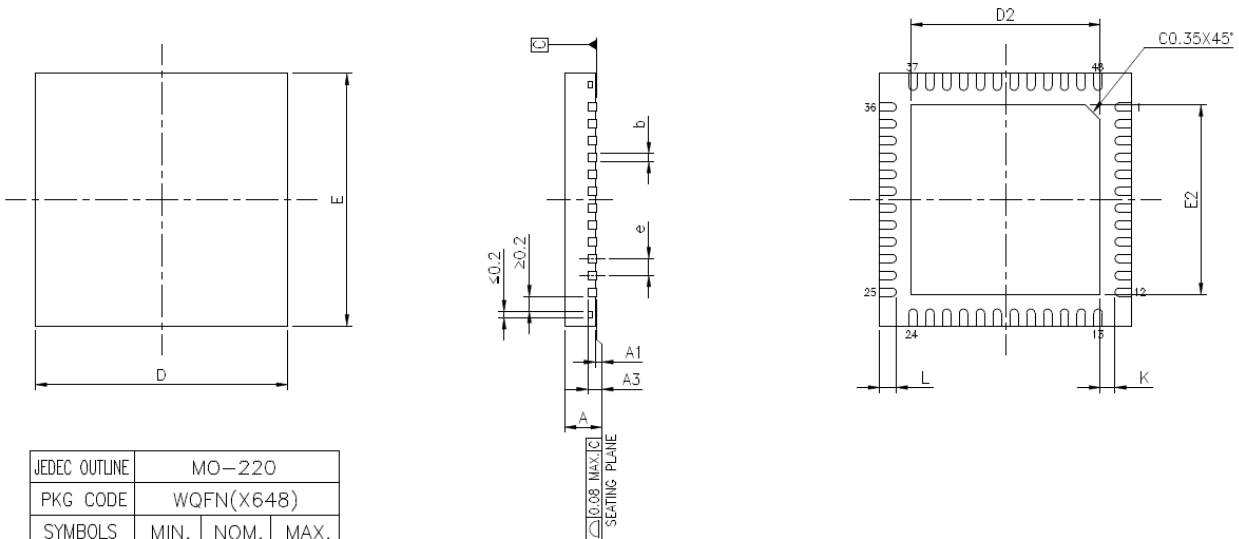
Symbol	Parameter	Conditions	Min	Typ.	Max	Units
T <sub>SKEW_DF</sub>	Input Differential Intra-Pair Skew	—	—	—	110	ps
T <sub>SKEW_CM</sub>	Input Common-mode Intra-Pair Skew	—	—	—	110	ps
F <sub>RXC</sub>	Common mode Input Clock	—	25	—	75	MHz
T <sub>RXC</sub>	Common mode Input Clock Period	—	13.33	—	40	ns
T <sub>CLOCK_JIT</sub>	Common-mode Clock Jitter	—	—	—	0.3T <sub>BIT</sub> + 200	ps
T <sub>DATA_JIT</sub>	Differential Data Jitter Tolerance	—	—	—	0.4T <sub>BIT</sub> + 88.88	ps

Table 6 TMDS Input Timings

## 3. Packaging and Marking Specification

### Marking



**PACKAGE DIMENSION**
**QFN48**


JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X648)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VQFN	WQFN	UQFN	TQFN OPTION 1	TOFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
185X18* ML	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	V	X	(W)VJJE-1	V	V	—	—	—

**NOTES :**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

## 4. References

HDMI 1.4b Specification

HDCP 1.4 Specification