TEA1995T

GreenChip Synchronous Rectifier controller

Rev. 1.1 — 1 September 2014　Objective data sheet

1. General description

The TEA1995T is the first product of a new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies with adaptive gate drive for maximum efficiency at any load.

The TEA1995T is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It has two driver stages for driving the SR MOSFETs which are rectifying the outputs of the secondary transformer windings. The two gate driver stages have their own sensing inputs and operate independently of each other.

The TEA1995T can also be used in multi-output flyback converters with the SR MOSFET placed at the low side.

The TEA1995T is fabricated in a Silicon On Insulator (SOI) process.

2. Features and benefits

2.1 Efficiency features

Adaptive gate drive for maximum efficiency at any load.
Supply current in no-load operation below 200μA.

2.2 Application features

Very wide supply voltage range from 4.5V to 40V.
Dual Synchronous Rectification for LLC resonant in SO8 package.
Synchronous Rectification for multi-output flyback converters.
Supports 5V operation with logic level SR MOSFETS.
Differential inputs for sensing the drain and source voltage of each SR MOSFET.

2.3 Control features

SR control without minimum on-time.

Adaptive gate drive for fast turn-off at the end of conduction.

Under voltage lock out with active gate pull-down.

3. Applications

The TEA1995T is intended for resonant power supplies. In such applications, it can drive two external Synchronous Rectifier MOSFETs which replace diodes for the rectification of the voltages on the two secondary windings of the transformer.
It can be used in all power supplies needing high efficiency, like:

- Adapters
- Power supplies for desktop PC and all-in-one PC
- Power supplies for television
- Power supplies for servers

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1995T/N1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

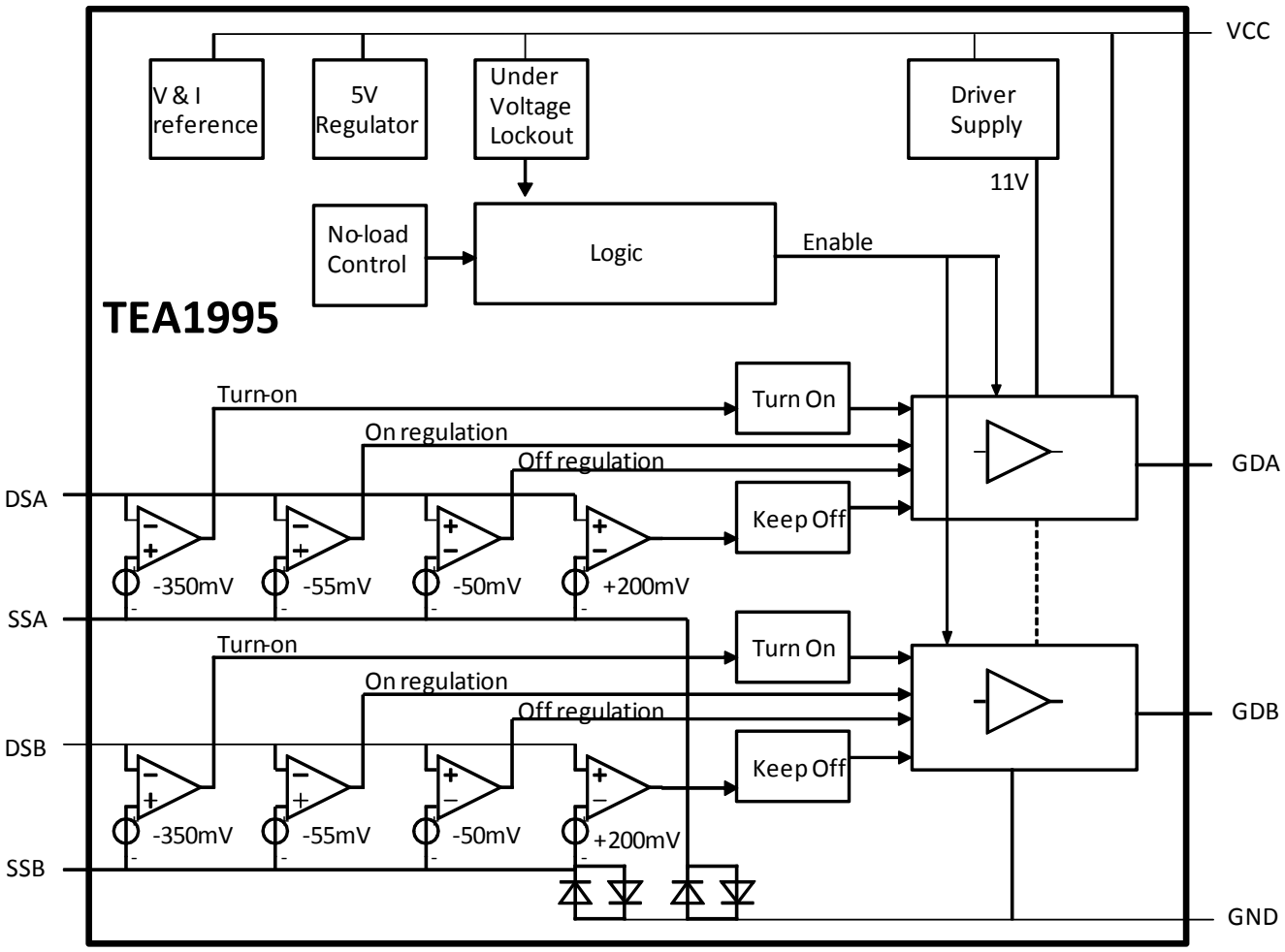


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

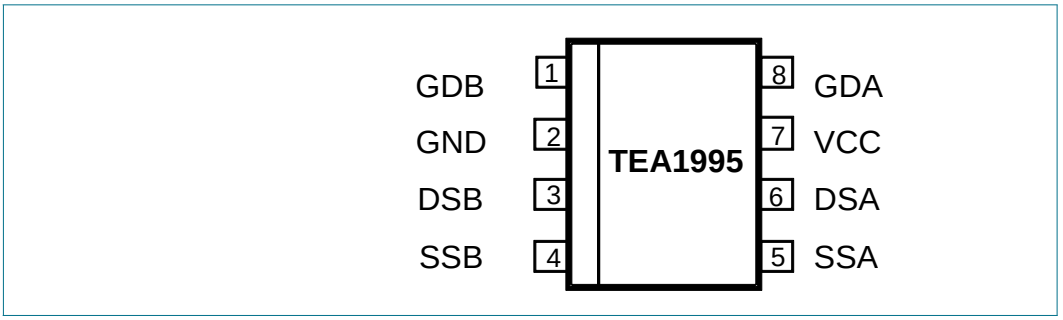


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GDB	1	gate driver output MOSFET B
GND	2	ground
DSB	3	drain sense input for synchronous timing MOSFET B
SSB	4	source sense input MOSFET B
SSA	5	source sense input MOSFET A
DSA	6	drain sense input for synchronous timing MOSFET A
VCC	7	supply voltage
GDA	8	gate driver output MOSFET A

7. Functional description

7.1 Introduction

The TEA1995T is a controller IC for Synchronous Rectification to be used in resonant applications. It can drive two Synchronous Rectifier MOSFETs on the secondary side of the central tap transformer winding. A typical configuration is shown in Figure 3.

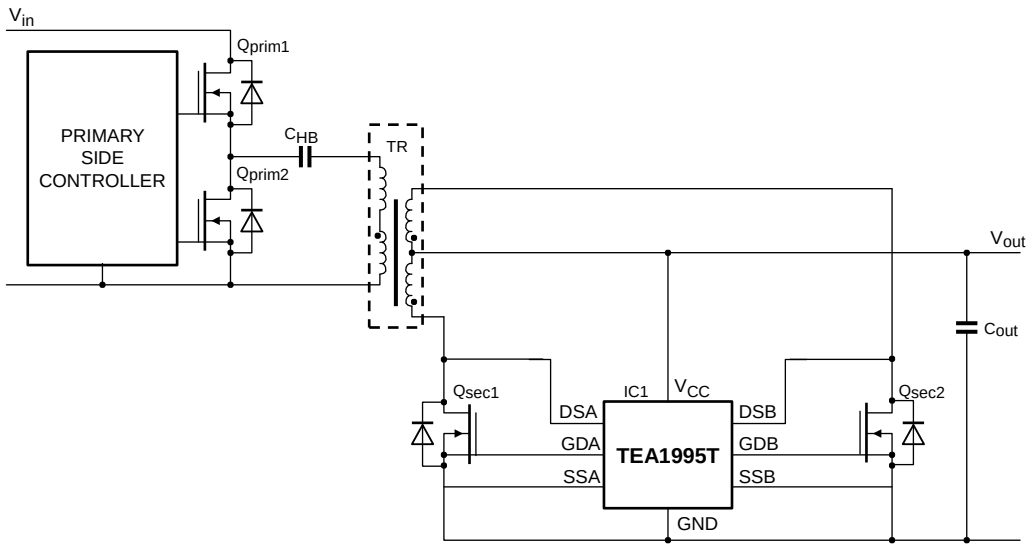


Fig 3. TEA1995T: typical configuration

7.2 Start-up and UnderVoltage LockOut (VCC pin)

The IC leaves the UVLO state and activates the Synchronous Rectifier circuitry when the voltage on the V_{CC} pin is above $V_{startup}$ (4.5 V typical). When the voltage drops below 4.2 V (typical), the UVLO state is reentered and the SR MOSFET gate driver outputs are actively kept low.

7.3 Drain sense (DSA and DSB pins)

The drain sense pins are input pins capable of handling input voltages up to 100V. At positive drain sense voltage the gate driver is in off-mode with pulled down gate driver pin (pin GDA or GDB). At negative drain sense voltage the IC enables the Synchronous Rectification by sensing the drain source differential voltage.

7.4 Synchronous rectification (DSA, SSA, DSB and SSB pins)

The IC senses the voltage difference between the drain sense (pins DSA and DSB) and the source sense (pins SSA and SSB) connections. This drain source differential voltage of the SR MOSFET is used to drive the gate of the SR MOSFET.

When this absolute voltage difference is lower than 350mV ($V_{act(drv)}$), the corresponding gate driver output turns on the external SR MOSFET. When the external SR MOSFET is switched on, the absolute voltage difference between the drain and the source sense connections will drop below 350mV ($V_{act(drv)}$) and the turn on phase will be followed by the regulation phase.

In the regulation phase the IC regulates the difference between the drain and the source sense inputs to an absolute level of 55mV. When the absolute difference is higher than 55mV ($V_{reg(drv)}$), the gate driver output increases the gate voltage of the external SR MOSFET until the 55mV level has been reached. The SR MOSFET will not switch off at low current and the IC operates without minimum on-time.

When the absolute difference is lower than 50mV the gate driver output decreases the gate voltage of the external SR MOSFET; the voltage waveform on the gate of the SR MOSFET follows the waveform of the current through the SR MOSFET. The SR MOSFET will be switched off quickly when the current through the external SR MOSFET reaches zero.

After switching-off of the SR MOSFET the drain voltage will rise, for a drain voltage above 200mV the gate of the SR MOSFET will be kept off by a low ohmic gate pull-down of 4 ohm.

7.5 Gate driver (GDA and GDB pins)

The gate driver circuit charges the gate of the external SR MOSFET during the rising part of the current and the driver circuit discharges the gate during the falling part of the current. The gate driver has a source capability of typically 1A and a sink capability of typically 1.2 A. This allows fast turn-on and fast turn-off of the external SR MOSFET.

The maximum output voltage of the driver is limited to 12 V. This high output voltage drives all MOSFET brands to the minimum on-state resistance.

In applications where the IC is supplied with 5V the maximum output voltage of the driver is limited to 5V and logic level SR MOSFETS can be used.

During start-up conditions ($V_{CC} < V_{startup}$) and UVLO the driver output voltage is actively pulled low.

7.6 Source sense (SSA and SSB pins)

The IC is equipped with additional source sense pins (SSA and SSB). These pins are used for the measurement of the drain-to-source voltage of the external SR MOSFET. The source sense input should be connected as close as possible to the source pin of the external SR MOSFET to minimize errors, caused by voltage difference on PCB tracks due to parasitic inductance in combination with large dI/dt values.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		−0.4	+40	V
$V_{sense(D)A}$	drain sense voltage A		−0.8	+100	V
$V_{sense(D)B}$	drain sense voltage B		−0.8	+100	V
$V_{sense(S)A}$	source sense voltage A		−0.4	+0.4	V
$V_{sense(S)B}$	source sense voltage B		−0.4	+0.4	V
Currents					
$I_{I(DSA)}$	input current on pin DSA		-	-	mA
$I_{I(DSB)}$	input current on pin DSB		-	-	mA
$I_{I(SSA)}$	input current on pin SSA		-	-	mA
$I_{I(SSB)}$	input current on pin SSB		-	-	mA
General					
P_{tot}	total power dissipation		-	0.5	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
ElectroStatic Discharge voltage (ESD)					
V_{ESD}	electrostatic discharge voltage	class 2			
		human body model [1]	-	2000	V
		charged device model	-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	140	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 12 V; $C_{GDA/B}$=10nF (capacitor between GDA and GND and between GDB and GND), all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage management (pin V_{CC})							
V_{start}	start voltage				4.5		V
V_{hys}	hysteresis voltage		[1]		0.3		V
$I_{CC(oper)}$	operating supply current	Energy save, $V_{DSA/B}$=12V, $V_{SSA/B}$=0V			170		uA
		Normal operation, $V_{DSA/B}$=V_{SSA}=0V			1.6		mA
Synchronous rectification sense input (pins DSA/SSA and pins DSB/SSB)							
$V_{act(drv)}$	driver activation voltage	$V_{sense(S)A/B}$ = 0 V			−350		mV
$V_{reg(drv)}$	driver regulation voltage	$V_{sense(S)A/B}$ = 0 V;			−55		mV
$V_{deact(drv)}$	driver deactivation voltage	$V_{sense(S)A/B}$ = 0 V;	[2]	-	−50	-	mV
$V_{keepoff}$	keep-off voltage	$V_{sense(S)A/B}$ = 0 V		-	0.2	-	V
$t_{d(act)(drv)}$	driver activation delay time	$V_{sense(S)A/B}$ = 0 V; Normal operation; time from step on $V_{DSA/B}$ (2V to -0.5V) to rising of $V_{GDA/B}$		-	100	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	$V_{sense(S)A/B}$ = 0 V; Normal operation; time from step on $V_{DSA/B}$ (-0.5V to 2V) to falling of $V_{GDA/B}$		-	30	-	ns
Gate driver (pins GDA/GDB)							
I_{source}	Peak source current	V_{CC} = 5 V; pins GDA/GDB = 2 V		-	−0.4	-	A
		V_{CC} = 12 V; pins GDA/GDB = 2 V		-	−1.0	-	A
I_{sink}	Peak sink current	V_{CC} = 5 V; pins GDA/GDB = 2 V		-	0.5	-	A
		V_{CC} = 12 V; pins GDA/GDB = 2 V		-	1.2	-	A
$R_{sink(uvlo)}$	Gate pull down at start	Vcc=3.5V; $I_{GDA/B}$=100mA		-	10	-	Ohm
$R_{sink(off)}$	Gate pull down in off state	$V_{DSA/B}$=2V; $I_{GDA/B}$=100mA		-	4	-	Ohm
$V_{o(max)}$	maximum output voltage				11		V
Switching							
$f_{sw(max)}$	maximum switching frequency			500	-	-	kHz

[1] The V_{CC} under voltage lockout voltage is $V_{start} - V_{hys}$.

[2] The $V_{deact(drv)}$ level is always above the $V_{reg(drv)}$ level. Levels will never cross for prevention against simultaneous charging and discharging of the gate of the SR MOSFET.

11. Application information

A resonant switched mode power supply with the TEA1995T consists of a primary side half bridge, a transformer, a resonant capacitor and an output stage. In the output stage SR MOSFETs are used to obtain low conduction loss rectification. These SR MOSFETs are controlled by the TEA1995T.

The gate drive voltage for the Synchronous Rectifier switch is derived from the voltage difference between the corresponding drain sense and source sense pins.

Special attention should be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for gate drive voltage. Wrong measurement results in less efficient gate drive due to too low or too high gate voltage. The connections to these pins should not interfere with the power wiring. The power wiring conducts currents with high dI/dt values. This can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source sense pins make it possible to sense the source voltage of the external MOSFETs directly, without having to use the current carrying power ground tracks for this.

11.1 Application diagram resonant application

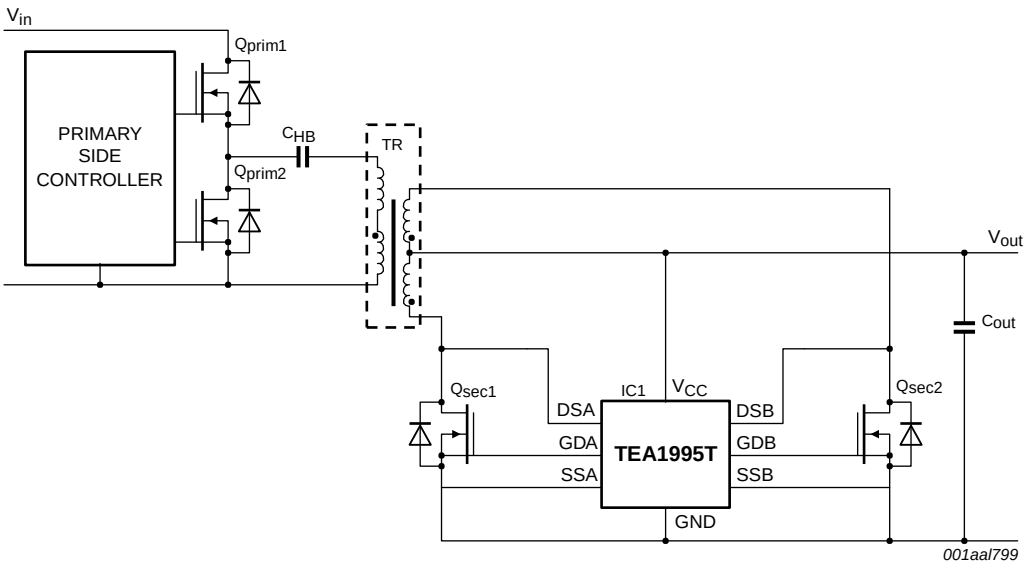


Fig 5. Typical resonant application with TEA1995T

11.2 Application diagram multi-output flyback application

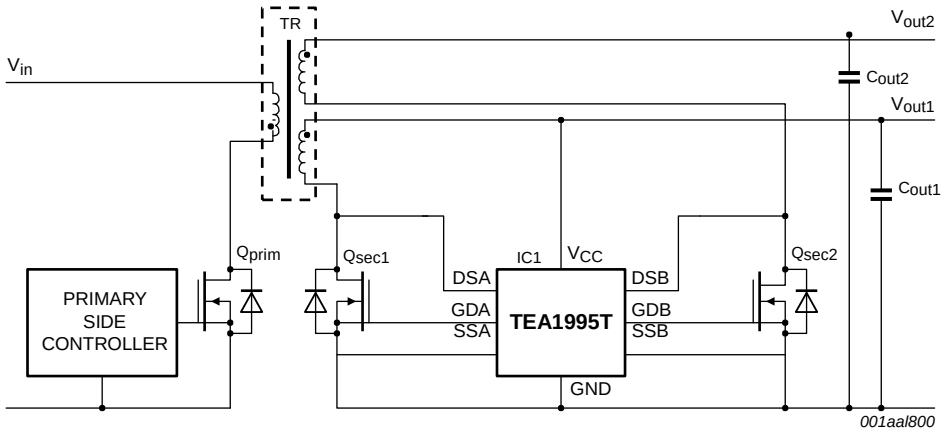
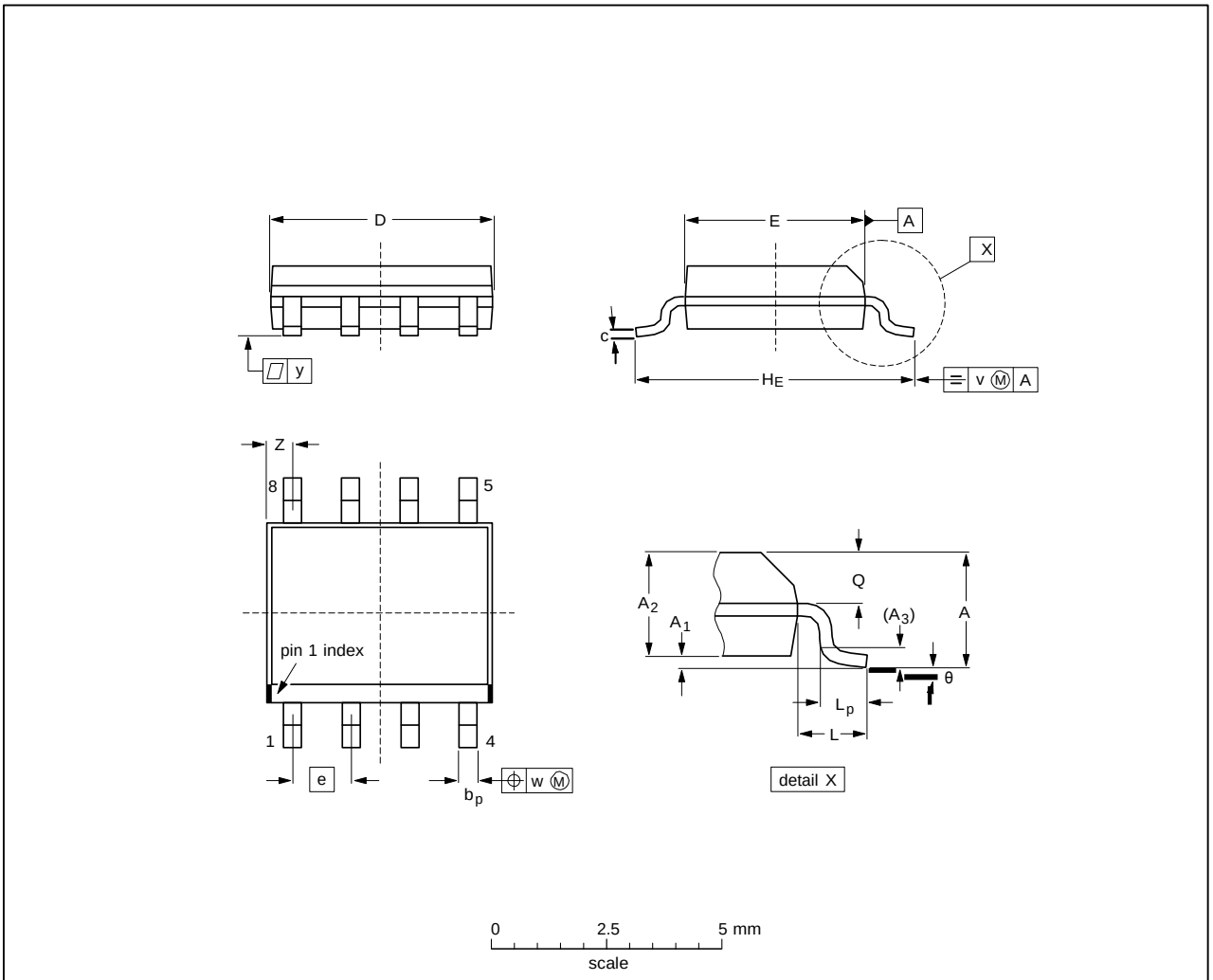


Fig 6. Multi-output flyback application with TEA1995T

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT096-1 (SO8)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1995T v.1.1	20140901	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

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