Optimizing Single-Stage Power Factor Correction

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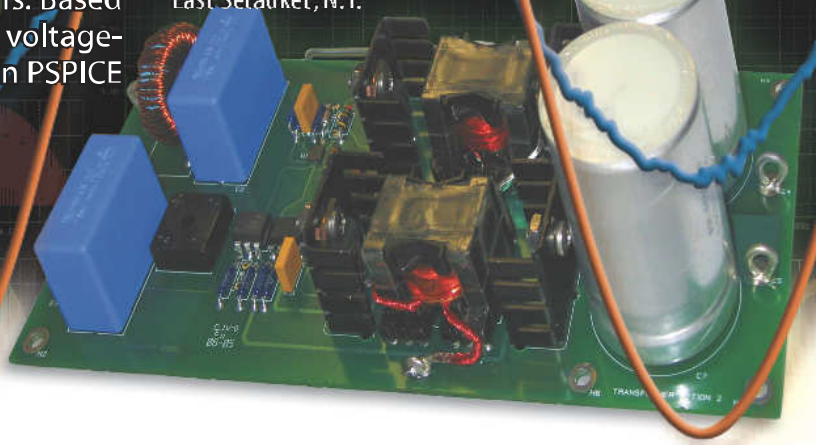
A comparison of four distinct PFC topologies reveals their inherent design tradeoffs. Based on these comparisons, a two-phase voltage-mode flyback converter is simulated in PSPICE and prototyped.



Traditional power factor corrected designs utilize a boost topology to accomplish the input power factor correction (PFC) function. The boost topology results in a nonisolated, high-voltage (approximately 400-V) dc output. This high-voltage output powers a dc-dc converter, which provides the required output voltages and input-to-output isolation.

Many new integrated circuits are being developed for the purpose of PFC control. Some of these new controllers incorporate both the PFC controller and a dc-dc controller within a single chip, while others offer critical-mode (also called transition-mode) control. The critical conduction mode eases the reverse-recovery stress that is seen by the boost diode.

The boost topology offers several benefits, primarily a very high operating efficiency. Because the boost converter only has to switch the difference between the input voltage and the output voltage, this topology generally results in small magnetic elements and efficiencies higher than 95%, with the voltage being somewhat proportional to the input voltage.

The boost topology also has some negatives such as the inability to short-circuit protect the boost stage. Another drawback is the high stress on the boost diode that results from very high dV/dT at a high applied voltage during the reverse-recovery period. The boost topology also exhibits a large inrush current unless an inrush limiter circuit is included, which adds to the complexity of the design. Additionally, the boost topology generally requires a dc-dc converter, which in turn requires the power to be switched twice and pushes up the parts count because of the two stages.

In many applications, it is preferable to perform the PFC and the isolation within a single converter stage. This is presently common in low-power applications up to about 40 W using SEPIC and discontinuous-conduction-mode flyback topologies. Four topologies may be used to provide a 28-V, 200-W output from a single-phase 400-Hz input. The four topologies include the critical-conduction isolated SEPIC, the continuous-conduction isolated SEPIC, the single-phase voltage-mode flyback and the multiphase (two-, three- or four-phase) voltage-mode flyback.

While all four of these converter topologies can accommodate a universal input range, the major considerations for this article are overall operating efficiency, fundamental input conducted emissions, output capacitor stress, reliability and relative cost. **Table 1** summarizes the key performance criteria. The performance of each of the topologies is assessed at a nominal 115-V_{RMS}, 400-Hz input voltage. The values shown in the **table** are from calculation or PSPICE simulation. EMA Design Automation supplied the PSPICE software and Power IC Model Library used for the simulation (www.EMA-EDA.com).

While the performance of the critical conduction boost is outstanding, it still needs an isolated dc-dc converter, which consumes watts and dollars, losing much if not all of

	Critical Conduction Boost*	Critical Conduction Isolated SEPIC	Continuous Conduction Isolated SEPIC	Voltage-Mode Flyback	Two-Phase Voltage-Mode Flyback	Four-Phase Voltage-Mode Flyback
Efficiency	94.6%	91.2%	89.3%	86.7%	87.7%	88.3%
Emissions	170 mA at 106 kHz	247 mA at 100 kHz	667 mA at 50 kHz	1.69 A at 100 kHz	0.826 A at 200 kHz	0.233 A at 400 kHz
Distortion	1.54%	7.21%	4.34%	1.05%	1.09%	1.11%
Power Factor	0.997	0.998	0.999	0.998	0.997	0.998
Ripple Current	1.108 A_{RMS}	12.30 A_{RMS}	11.3 A_{RMS}	13.6 A_{RMS}	8.09 A_{RMS}	6.07 A_{RMS}

* Still required a dc-dc converter for isolation.

Table 1. *Comparison of different topologies for the 28-V, 200-W power supply.*

its advantage. The SEPIC topology was interesting, but with simple control circuitry, it results in relatively high distortion and also the output capacitor ripple current is very high. The ripple current is significant because the output capacitors are expensive and have high failure rates. Topologies that reduce the number of output capacitors required or the output ripple current are advantageous for that reason.

Taking all of these requirements into account, we chose one of the four topologies as the basis for the detailed single-stage PFC converter design discussed in this article. A prototype of this design was built and evaluated for performance. Cornell Dubilier Capacitors (www.cde.com) assisted with the design and supplied the high ripple-current, low-ESR capacitors. Champs Technologies (www.champs-tech.com) provided detailed magnetics designs and samples for the prototypes.

Two-Phase Flyback

The topology selected for this application is the two-phase voltage-mode flyback. The multiphase flyback offers lower RMS currents in the input and output by effectively increasing the duty cycle. The schematic used for PSPICE simulation of the topology is shown in **Fig. 1**, while simulation results are shown in **Figs. 2** and **3**.

The two-phase voltage-mode flyback offers a significant ripple current reduction in the output capacitor, high efficiency and reasonable cost. The four-phase solution might be more attractive at higher power levels and there are three- and four-phase buck controllers available, but such a design appears overly complex for the 200-W power level.

The discontinuous-mode flyback naturally provides PFC using standard voltage-mode control circuits. The peak

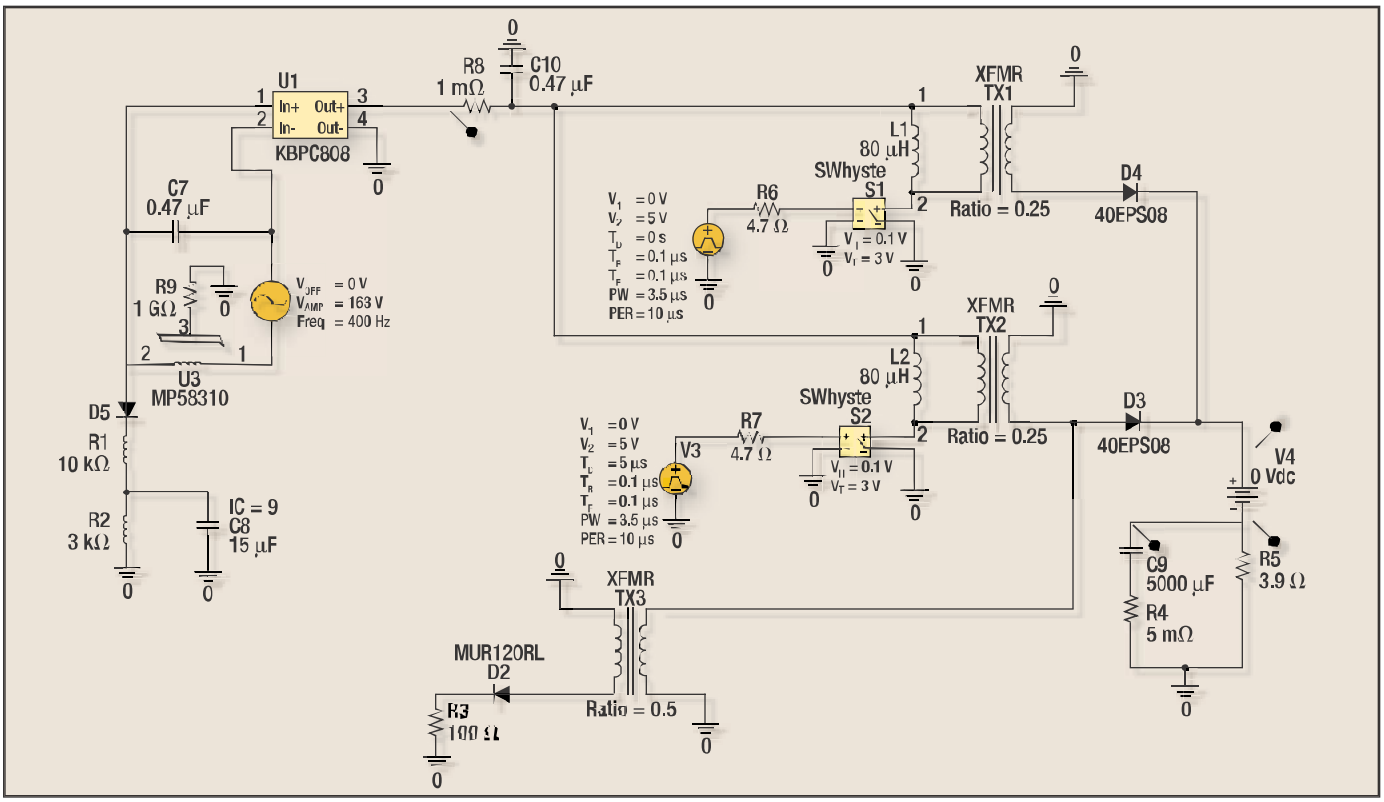


Fig. 1. *A PSPICE simulation of the two-phase voltage-mode flyback converter uses the above schematic values. Models used in the simulation of this and the other converter topologies can be found in the "Power IC Model Library" for PSPICE (EMA Design Automation, www.EMA-EDA.com).*

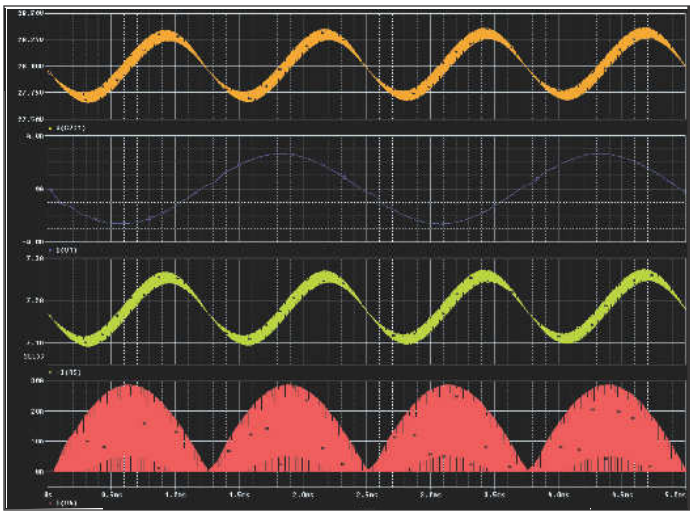


Fig. 2. *PSPICE transient simulation results. The waveforms from top to bottom are the output voltage, input current, output current and secondary-switched current.*

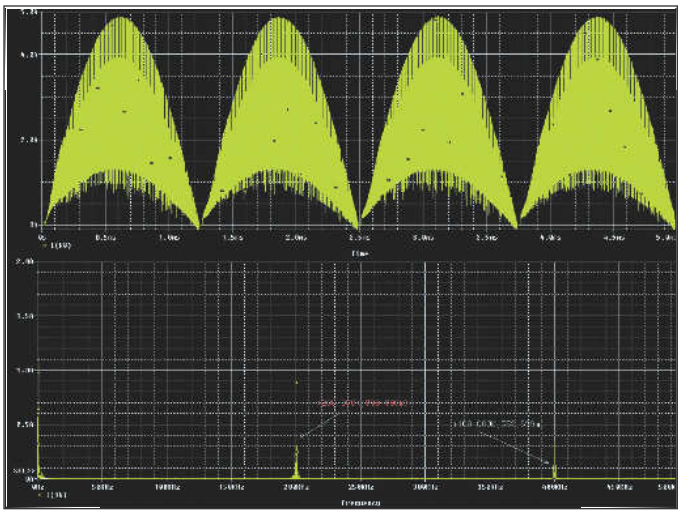


Fig. 3. *Simulated Fourier response for the two-phase design. The upper trace shows the switching current presented to the input filter and the lower trace shows the fundamental and first harmonic current presented to the input filter.*

primary current (I_p) of the flyback, along with the expected efficiency, can be calculated as follows:

$$I_p = \frac{V_{IN}}{L_p} T_{ON}$$

where V_{IN} is the input voltage applied at the top of the power transformer (rectified sine wave), L_p is the primary inductance and T_{ON} is the on-time of the MOSFET. The power delivered to the load is:

$$P_{IN} = \frac{1}{2} L_p I_p^2 \text{Freq}$$

where Freq is the switching frequency. Substituting for I_p and substituting for P_{IN} gives the input resistance.

$$R_{IN} = 2\frac{L_p}{T_{ON}^2 \text{Freq}}.$$

Therefore, it can be seen that for a fixed primary inductance, fixed on-time and fixed frequency, the input appears resistive. If L_p = 80 µH, T_{ON} = 4.5 µsec and Freq = 100 kHz, then R_{IN} = 79.012 Ω. This relationship determines the maximum power available at minimum load. The equation for R_{IN} also clearly shows that if T_{ON}, L_p and Freq are all constant, then the input resistance is constant, defining PFC. The distortion is then based primarily on the errors (variations) in L_p, T_{ON} and Freq within a cycle.

$$V_{IN}(t) = V_{INrms}\sqrt{2}\sin(2\pi \times 60t).$$

For P_{OUT} = 200 W, V_{IN} = 115 V_{RMS} and V_{OUT} = 28 V:

$$P_{IN} = \frac{P_{OUT}}{\eta}.$$

If the efficiency is assumed to be 90%, then η=0.9 and P_{IN}=222.222 W. The average current then becomes:

$$I_{IN}(t) = \frac{P_{IN}}{\int_0^{\frac{1}{120}} 115\sqrt{2}\sin(2\pi \times 60t)120\,dt}$$

or $I_{IN}(0.004333)$ = 2.195 A.

If we assume that there are N phases, then the input power is split evenly between each of the N phases. If N = 2, then:

$$P_N = \frac{P_{IN}}{N}$$

and $P_N \times 2 = 0.5\, L_p I^2_{PKsw} \times \text{Freq}$.

For $L_{PRI} = N \times 40 \times 10^{-6}$ and Freq = 100×10^3 Hz,

$$I_{PKsw} = \frac{2}{L_{PRI}\text{Freq}}\sqrt{L_{PRI}\text{Freq}P_N},$$

which gives I_{PKsw} = 7.538 A and

$$T_{ON} = \frac{L_{PRI}I_{PKsw}}{V_{INrms} \times 1.414} = 3.708 \times 10^{-6}\ \text{s and}$$

Duty = T_{ON}, Freq = 0.371. The RMS inductor current can be estimated as:

$$I_{RMSsw} = \sqrt{\frac{\text{Duty}}{3}}\frac{\sqrt{2}}{2} I_{PKsw} = 1.874\ \text{A}.$$

Assessing the MOSFET switch losses with $T_C = 50 \times 10^{-9}$ s and $R_{DS(ON)}$ = 0.4 Ω.

$$P_{FETsw} = 120\int_0^{\frac{1}{120}} \left(V_{INrms}\sqrt{2}\sin(2\pi \times 60t)\right) \times \left(I_{PKsw}\sin(2\pi \times 60t)\right)\frac{T_C \text{Freq}}{2}\,dt \times N,$$

giving P_{FETsw} = 3.065 W.

The conduction losses are defined by:

$$I_{FETrms} = \sqrt{\frac{\text{Duty}}{3}}\frac{\sqrt{2}}{2} I_{PKsw}\ ; \text{therefore,}$$

$P_{FETcond} = I^2_{FETrms} \times R_{DS(ON)} \times N$, where $P_{FETcond}$ = 2.809 W.

The input rectifier losses are a result of the forward voltage, V_{Fin}, and the input current, V_{Fin} = 0.88 V:

$$P_{RECT_{IN}} = 2\frac{V_{Fin}P_{IN} \times 1.1}{V_{INrms}}$$

and the output rectifier loss is V_{Fout} = 0.85 V:

$$P_{RECTout} = V_{Fout}\frac{P_{OUT}}{V_{OUT}} = 6.071\ \text{W}$$

$P_{XFMR} = P_{OUT} \times 2.656\%$.

The transformer leakage inductance losses are also dissipated. With a measured leakage inductance of 1.5 µH, the leakage power is calculated as follows:

$$L_{LEAKAGE} = 0.75 \times 10^{-6} \times N$$

$$P_{LEAKAGE} = L_{LEAKAGE} I^2_{PKsw} Freq \frac{2}{\pi} N$$

$I_{RMScap} = 8.09$; $ESR_{CAP} = 0.27$; and $N_{CAPS} = 2$

$$P_{CAP} = I^2_{RMScap} \frac{ESR_{CAP}}{N_{CAPS}}$$

$$P_{LOSS} = P_{XFMR} + P_{RECTout} + P_{RECTin} + P_{FETcond} + P_{FETsw} + P_{LEAKAGE} + P_{CAP}$$

$P_{LOSS} = 28.875$ W

$$Efficiency = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Efficiency = 0.874.

Magnetics Design

The design approach for an isolated flyback transformer for PFC is similar to a discontinuous-mode (DCM) flyback transformer. The difference is that, for the PFC application, the input voltage and current vary more than one-half of the cycle of the ac input.

Optimizing the transformer requires an accurate computation of the winding and core losses. The method shown in reference 3 computes the Fourier components of the voltage waveform (across the primary) and then computes the core loss for each harmonic of the waveform. The core loss curves and equations supplied by most core manufacturers are for sine wave excitation, making this an ideal method. Similarly, the Fourier components of the current waveforms for the primary and secondary are derived and the winding losses for each harmonic are then computed. This allows a formulaic approach using skin and proximity effects to accurately predict the winding losses. Most traditional methods for DCM do not go into this level of detail because a first-order approach is often satisfactory.

Design equations must be written and the analytical results compared to empirical data on efficiency and temperature rise. In our two-phase example, each transformer provides half the output power, or 100 W with a switching frequency of 100 kHz. Consequently, $L_p = 80 \times 10^{-6}$ H, $I_{PKpri} = 7.5$ A, $I_{PRIrms} = 2.6$ A, transformer turns ratio = 0.25 and $I_{SECrms} = 7.65$ A.

Two transformer design choices were selected for evaluation: a PQ2620 size ferrite core and a standard PL58 size planar ferrite core. Both transformers were constructed. Results of the PQ calculations are shown in **Table 2**. The leakage inductance of the transformer was measured to be 1.5 µH at 100 kHz. A relative cost comparison of the two choices is also shown.

The PQ core finds worldwide usage currently in existing

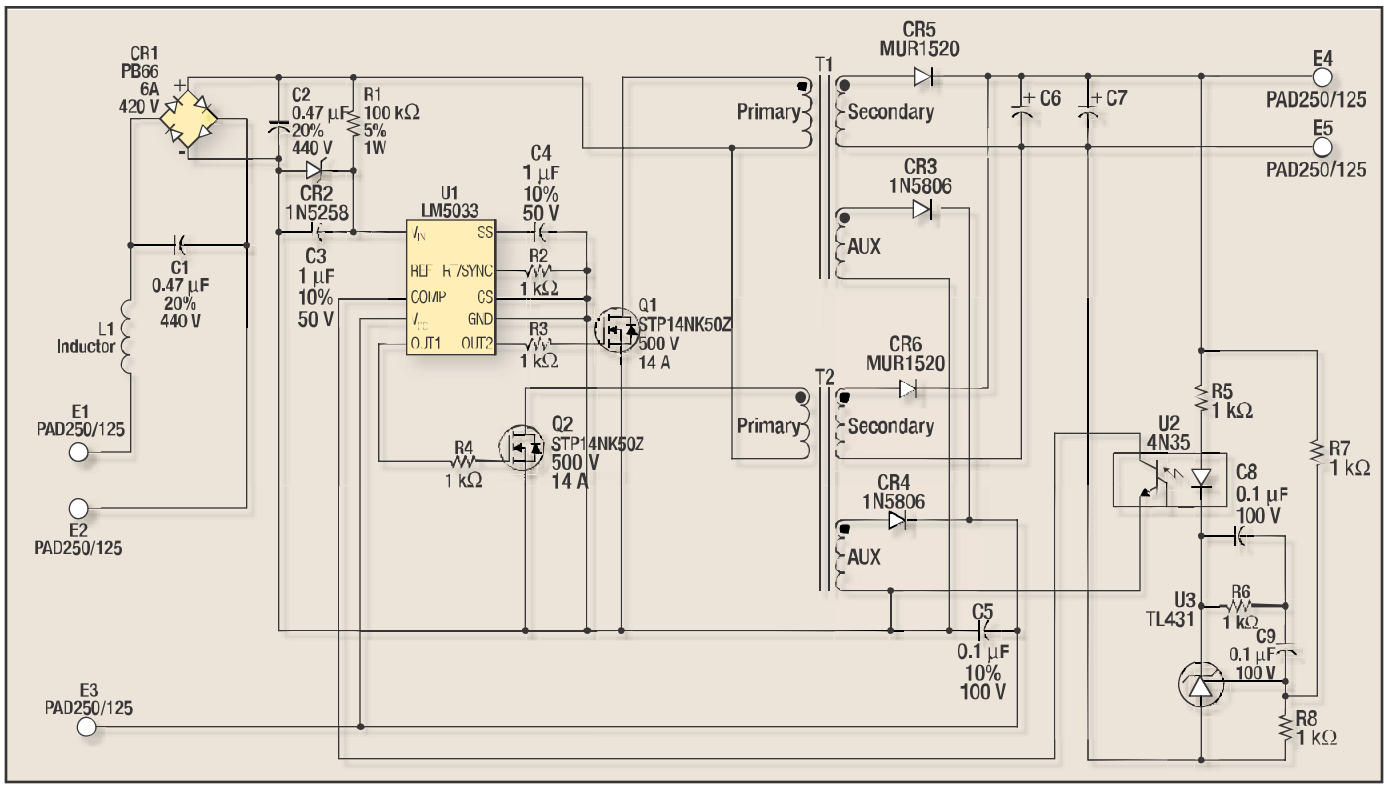


Fig. 4. *Schematic of the two-phase voltage-mode flyback converter.*

off-line ac-dc power supplies resulting in a very low cost. The planar cost is directly related to the number of boards or layers (lead frame or pc board) required to achieve the design requirements. Applications more amenable to planar designs usually occupy niches in telecom, "bricks," servers and high current/power. The result is that the PQ core is substantially less expensive than the planar counterpart, due to the high production volume of the part. For that reason, this article concentrates on the PQ design, though both were built for evaluation.

The first planar design resulted in very high leakage inductance. Additional work will be done to improve the leakage inductance so that the planar can be properly evaluated. The planar design has the benefits of very low profile and very low labor cost.

Fig. 4 shows the actual schematic for the two-phase voltage-mode flyback design that was constructed. The design utilized a National Semiconductor LM5033, 100-V push-pull voltage-mode pulse-width modulated (PWM) controller. This controller was selected for several reasons. It has low initial operating current and up to 100-V input. It also provides high-current output drivers and a wide operating temperature range. A final benefit is that it is designed for applications using optically coupled feedback.

The reliability of the supply is almost totally dependent on the output capacitor. The failure rate of the output capacitor is, in turn, dramatically affected by the ripple current. For the selected CDE capacitor, failure rates vary from more than 100,000 hours to under 10,000 hours as the ripple current goes from 0% of the rated value to 150% of the rated value.

Core	Width (mm)	Length (mm)	Height (mm)	Core Area (mm^2)	Volume (mm^3)
PQ2620	19	27.3	20.2	1.09	5.47
PL58	20	25	11	0.75	3.2
Core	**Secondary Cu Loss (W)**	**Gap Loss (W)**	**Core Loss (W)**	**AC Loss (W)**	**Total Loss (W)**
PQ2620	0.3	0.78	0.44	1.136	2.656
Core	**Cost per 1000 units**	**Cost per 10,000 units**	**Cost per 50,000 units**	**Cost per 100,000 units**	**Cost per 1,000,000+ units**
PQ2620	$2.20	$1.35	$0.675	$0.655	$0.62
PL58	$3.80	$3.20	$2.50	$1.80	$1.50

Table 2. *PQ ferrite core versus PL planar ferrite core as transformer elements.*

The math for the capacitor ripple current shows the theoretical minimum current for the line frequency component, which is what we would get if we had an infinite number of stages (no high-frequency contribution):

P_{OUT} = 200 W and V_{OUT} = 28 V

$I_{OUT} = \frac{P_{OUT}}{V_{OUT}}$ and $I_{PK} = I_{OUT}\frac{\pi}{2}$, making I_{PK} = 11.22 A.

The current in the output capacitor at the line frequency is:

$I_{CAP}(t) = I_{PK} \times \sin(t) - I_{OUT}$

and the RMS capacitor current at the line frequency is:

$$I_{RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(I_{OUT}\frac{\pi}{2}\sin(t) - I_{OUT}\right)^2 dt} = 3.453\ A.$$

Number of Phases	Output Caps Utilized	Ripple per Cap (A_{RMS})	Failure Rate for Output Caps (fpmh)	Unit Failure Rate (fpmh)	Unit MTBF (hr)
1	3	4.53	9.346	29.954328	33384.16
2	2	4.05	8.333	18.782362	53241.44
3	2	3.2	6.667	15.650395	42386.54
4	1	6.07	13.33	15.849429	63093.76

Table 3. *Calculation of the failure rate and MTBF performance versus the number of phases.*

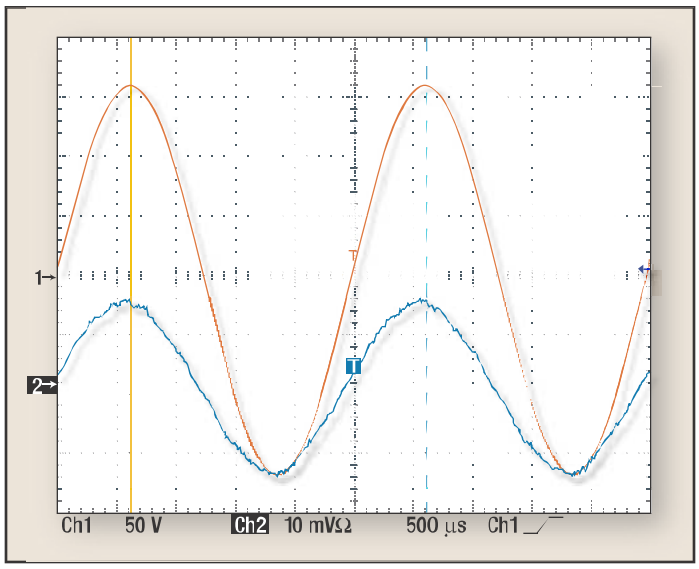


Fig. 5. *Bench results for the 200-W PFC converter with the PQ2620 magnetics. The upper trace shows the input voltage at 50 V/div and the lower trace is the input current at 2 A/div.*

Of course, in addition to this current, there is also the high-frequency switching component; however, this is the minimum theoretical limit.

As the number of phases is increased, the capacitor ripple current will decrease asymptotically toward this theoretical minimum. **Table 3** shows the mean-time-before-failure (MTBF) calculations for one-, two-, three- and four-phase versions of the flyback supply.

Parameter	Measured	Calculated
Efficiency	87.4%	86.9%
Distortion	1.03%	1.03%
Power Factor	0.997	0.997

Table 4. *Test data for two-phase voltage-mode flyback.*

In the two- and three-phase versions, two capacitors were required. The number of capacitors must be sufficient to handle the output capacitor ripple current, with adequate derating to improve the reliability. While the four-phase approach would further reduce the number of output capacitors, it was decided that the two-phase solution was adequate for this power level. The four-phase solution would require a more elaborate—and expensive—control circuit.

Since the output capacitor is also the most expensive component and almost solely responsible for the MTBF, its failure rate is more than 500 times that of any other component in the system, the number of phases must be carefully assessed for each application.

Fig. 5 shows the input voltage and current waveforms. A Voltech PM100 power analyzer and Elgar model 1001B were used in the testing of the two-phase flyback supply. The power analyzer is accurate to 0.1% for voltage, 0.1% for current, 0.2% for power and 0.4% for THD. The Elgar distortion limit is 0.6%, making it hard to measure the expected 1% distortion.

The measured performance for the final converter design is in excellent agreement with the calculated and simulated results. **Table 4** lists the measured and calculated values for converter performance using the PQ2620 transformers. Additional refinements of the power transformer may be feasible. The mathematical models having been proven out can now be used to evaluate specific design solutions using the multiphase flyback topology. **PETech**

References

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