Design and Implementation of Interleaved Vienna Rectifier with Greater than 99% Efficiency

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Abstract—In this paper, the design and implementation of a 3 kW, three-phase, two-channel interleaved Vienna rectifier with greater than 99% efficiency is presented. The operation principle of an interleaved Vienna rectifier is introduced, with particular attention paid to the circulating current generated by interleaving operation. The design procedure for achieving maximum efficiency is described. Methods for loss calculation and hardware implementation involved in the optimization procedure are introduced. Finally, a prototype of the proposed converter is constructed, which achieves 99.08% efficiency at nominal load.

I. INTRODUCTION

Active three-phase rectifiers are commonly used as a means of increasing efficiency and improving source current power quality as compared to passive rectifiers. Conventional 2-level 6-switch active boost rectifiers have been dominant in industry due to their simplicity. However, in order to achieve higher efficiency, 3-level converters are desirable due to lower switching voltage, thus allowing the use of lower voltage switches which usually present lower resistance and smaller junction capacitance [1]. Among the 3-level topologies, Vienna rectifiers have been widely used to achieve high efficiency [2, 3]. Several phase leg configurations for Vienna rectifiers have been proposed in [4-7]. In order to achieve minimum conduction loss, the configuration proposed in [6] is selected, where for each phase leg one diode is used for positive or negative rail clamping and two anti-series connected MOSFETs are used for middle point connection. With the use of SiC Schottky diodes, the reverse recovery loss from diodes in Vienna rectifiers can be eliminated, which further makes Vienna rectifier a promising topology in achieving high efficiency. Additionally, unlike other bi-directional topologies, there is no need to worry about transistor shoot-through failure modes [3]. Thus, in this paper, Vienna rectifier is selected as the basic converter unit for the interleaved system.

Paralleling switches or converters is a common practice to achieve higher efficiency and better thermal management. In such practices, interleaving the gate signals of several sub-converters instead of simply gating them simultaneously could further enhance efficiency and power density [8-11]. The cancellation effect among interleaved sub-converters allows smaller input filters. In other words, to achieve the same power quality with the same passive components, the switching frequency of each sub-converter in the interleaved systems can be lower, which lowers switching loss. Additionally, applying interleaving may reduce EMI filter size due to its cancellation effect among sub-converters [12]. Thus, an interleaved Vienna rectifier, which merges the advantages of Vienna rectifier and interleaved systems in achieving high efficiency, will be discussed herein.

In this paper, the design of a 3 kW, three-phase, two-channel interleaved Vienna rectifier with greater than 99% efficiency is presented. The converter efficiency is optimized for 230 V, 360~800 Hz input voltage, 650 Vdc output voltage and 3 kW output power. The operation principle of the interleaved Vienna rectifier is presented in Section II. A unique issue of interleaved converters, circulating current, will be discussed in Section III. Section IV presents a comprehensive design procedure for an interleaved Vienna rectifier, including design flow chart, loss estimation for the converter, design guideline of inter-phase inductors and semiconductor selection. Finally, in Section V, converter prototype and experimental results are shown, validating the design procedure.

II. OPERATION OF INTERLEAVED VIENNA RECTIFIER

A. Topology Introduction

Fig.1 shows the interleaved Vienna rectifier topology studied in this paper. In this topology, $S_1, S_2, S_5, S_6, S_9, S_{10}$ and the diodes directly connected to these MOSFETs form a sub-converter that can operate independently as a Vienna rectifier. The other switches form the other sub-converter. The two corresponding phase legs in different sub-converters are connected together with an inter-phase inductor (shown as $L_{MA}, L_{MB}$ and $L_{MC}$ in Fig. 1). $L_A, L_B$ and $L_C$ are the input boost inductors for the converter. Two corresponding phase legs merged by the inter-phase inductor share the same boost inductor, e.g. phase leg constituted by $D_1, D_2, S_1, S_2$ and phase
leg constituted by $D_3$, $D_4$, $S_3$, $S_4$ are merged by inter-phase inductor $L_{MA}$ and share input boost inductor $L_A$.

B. Operation Principle

The Vienna rectifier is current-commutated. The devices participating in commutation are determined by current direction, e.g. if current $I_{A1}$ in Fig. 2 is positive, the commutation will take place between $D_1$ and $S_1$, $S_2$. As a result, the voltage potential at point $A_1$ with reference to the middle point of DC bus will be either half of DC bus voltage (with $S_1$, $S_2$ off) or zero (with $S_1$, $S_2$ on).

Each sub-converter in this topology operates independently as a Vienna rectifier. To operate the whole converter in interleaved manner, we can introduce a phase shift between the carriers of the two corresponding phases in different sub-converters. With the two sub-converters interleaved, some current distortion in each interleaved phase will cancel, i.e. the current peak (valley) in a certain phase will meet with the current valley (peak) in its counterpart, producing smoother current waveform seen from source side. As a result, to achieve the same input current quality (THD), the switching frequency of each sub-converter in an interleaved converter can be much lower than a paralleled converter with the same input boost inductance, which helps reduce switching loss.

III. CIRCULATING CURRENT IN INTERLEAVED CONVERTERS

Interleaving two sub-converters brings unwanted circulating current into the system [10, 13]. Circulating current is the current produced by voltage difference between interleaved phases. As shown in Fig. 2, the current flowing through input boost inductor is defined as $2I_d$. The common current flowing through each interleaved phase is $I_d$. And the difference between the two currents is defined as circulating current, $I_{cir}$. If point $A_1$ is clamped to positive rail by diode $D_1$ and $A_2$ is connected to middle point of DC bus by $S_3$ and $S_4$, the voltage difference between $A_1$ and $A_2$ will generate current ($I_{cir}$) circulating within the two phases. If the impedance between the two points is not large enough, the circulating current will not only create additional conduction loss but also impede the functionality of the converter. E.g. when $I_d$ is positive, point $A_1$ should be clamped to either positive rail by $D_1$ or middle point of DC bus by $S_1$ and $S_2$. However, if $I_{cir}$ is so high that $I_{cir} = I_d - I_{cir} < 0$, point $A_1$ will not be able to be connected to positive rail when $S_1$ and $S_2$ are off, instead, it will be clamped to negative rail, resulting in false modulation. Thus, circulating current in interleaved current-commutated converters should be well controlled.

The voltage difference between the two points is inevitable in interleaved converters. In each switching cycle, the voltage difference is predetermined by modulation scheme and working condition. Thus, a practical way to attenuate the circulating current is to increase the impedance between the two interleaved points (in this case, $A_1$ and $A_2$) at frequencies close to and above switching frequency. Adding coupled inductors (inter-phase inductors) between interleaved phases (like $L_{MA}$ for phase $A_1$ and $A_2$ in Fig. 2) can effectively
increase the impedance of the circulating loop while keeping minor influence on the common current \(I_A\) \[10\]. The design of inter-phase inductors will be discussed in Section IV.

### IV. DESIGN PROCEDURE, EFFICIENCY ESTIMATION AND CONVERTER IMPLEMENTATION

To achieve optimized efficiency while keeping reasonable converter size, an efficiency-oriented design procedure for interleaved Vienna rectifier will be presented and discussed in this section.

#### A. Converter Design Procedure

The design procedure is described graphically via the flow chart diagram in Fig. 3. This procedure starts with definition of converter specifications and standard. Power quality requirements for current harmonics are described in Table I. Total harmonic distortion should be under 10%. The next step is to select the proper modulation scheme for the converter (will be discussed in part B). Then, a sweeping program will be executed to find the optimized design. The sweeping program starts with switching frequency selection, after which all the passive devices, e.g. input boost inductors, inter-phase inductors and DC bus capacitors can be designed (mainly constrained by power quality standard) and their loss can be estimated accordingly. Several combinations of semiconductor devices are considered in this efficiency estimation and optimization. Under certain switching frequency, the conduction loss and switching loss from all combinations of semiconductor devices could be analytically calculated (loss model will be discussed in part C in this section). The semiconductor device selection achieving lowest loss will be the optimized design at this switching frequency. By sweeping for different switching frequencies, the relationship between optimized total loss, design of passive components and switching frequency can be analytically shown and we can find the optimized design that has highest efficiency with reasonable size. All the design details will be explicitly shown in the remaining part of this section.

#### B. Modulation

All modulation schemes applicable to Vienna rectifiers can be applied to the interleaved system because interleaved sub-converters generate their outputs independently. However, in order to achieve high efficiency, discontinuous-PWM (DPWM), which clamps one phase within every switching period, is preferable in this design. Ref. [14] has proposed and compared two DPWM schemes for Vienna rectifiers. One of these schemes (its vector selection is shown in Fig. 4) is adopted in this paper. The blue circle in the picture presents the track of the output voltage vector. To achieve phase clamping, for example, in area 1, vector \([p \, n \, n]\), \([p \, n \, m]\) and \([p \, m \, m]\) are selected for the lower part. Vector \([p \, m \, m]\), \([p \, m \, n]\) and \([p \, n \, n]\) are selected for the upper part. These selections ensure that phase \(A\) is clamped to positive rail when the desired output voltage vector is in area 1. It is worth noting that, in area 1, current in phase \(A\) is close to its maxima. Clamping phase \(A\) in this area would always be beneficial for switching loss reduction. In area 2, vector \([p \, m \, m]\), \([p \, m \, n]\) and \([m \, m \, n]\) are selected to ensure phase B is clamped to middle point, where current in phase B crosses zero. Thus, this scheme not only avoids switching around the maxima but also avoids switching around zero crossing of associated phase current.

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**TABLE I. CURRENT HARMONIC LIMITS**

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Odd Non Triplen Harmonics ((h = 5, 7, \ldots, 37))</td>
<td>(I_h = 0.3 I_{1/h})</td>
</tr>
<tr>
<td>Odd Triplen Harmonics ((h = 3, 9, 15, 21, \ldots, 39))</td>
<td>(I_h = 0.15 I_{1/h})</td>
</tr>
<tr>
<td>Even Harmonics 2 and 4</td>
<td>(I_h = 0.01 I_{1/h})</td>
</tr>
<tr>
<td>Even Harmonics &gt; 4 ((h = 6, 8, 10, \ldots, 40))</td>
<td>(I_h = 0.0025 I_{1/h})</td>
</tr>
</tbody>
</table>
C. Loss Estimation

Losses of the converter mainly come from semiconductor devices and passive components. In this loss estimation, conduction loss, switching loss and core loss has been carefully modeled.

Conduction loss is directly related to the resistance of the conductor and the RMS current flowing through the conductor. The RMS current in a certain component can be calculated mathematically or from simulations. Assuming that interleaved sub-converters evenly share the current, circulating current is well attenuated by the inter-phase inductors, and that skin effect and proximity effect are negligible with the use of Litz-wire for inductor windings, conduction loss is accurately modeled and calculated.

Switching of MOSFETs is a highly nonlinear procedure, making switching loss modeling and calculation a harder task. In this design, a revised model [15] developed from a linear model proposed in [16] is used. The circuit model used in this revised linear model is shown in Fig. 5. In this model, the gate charges of the MOSFET instead of the non-linear capacitances are used to calculate the turn-on and turn-off time due to the consistency of the charges in a wide voltage range. Common source inductors (L_s in Fig. 5) and the loss caused by charging the diode during its turn-off is considered. Transition of the drain-to-source current and voltage are assumed to be linear. Typically, there are four intervals in a switching procedure, which is shown in Fig. 6. The duration of each interval is determined by the driving circuits, parasitic and, most importantly, gate charge dominating the interval. To be more specific, the turn-on procedure is described below:

1) Gate voltage $V_g$ increases from zero to threshold voltage $V_{th}$. Gate charge needs to be provided by driver is $Q_{th}$. There is no switching loss from this interval;

2) Gate voltage $V_g$ increases from $V_{th}$ to $V_{pl}$, plateau voltage of the MOSFET. In [15], it is assumed that $V_{gs}$ stays at $V_{pl}$ in this interval while in this paper, the variation of $V_{gs}$ is considered, making it more accurate. At the same time, drain-to-source current rises to load current. Gate charge during this interval provided by gate driver is $Q_{gs1}$. Duration of this interval $t_r$ is given by:

$$ t_r = \frac{2R_g (Q_{gs1} + \frac{I_{load}}{L_s})}{2(V_{dr} - V_{th} - V_{pl})} $$

where $R_g$ is the gate resistor, $L_s$ is the common source inductance, $I_{load}$ is the load current and $V_{dr}$ is the gate driver output voltage;

3) Gate voltage $V_g$ stays at $V_{pl}$, which is caused by Miller Effect. Drain-to-source voltage begins to drop. Total charge needed is $Q_{gd}$ in datasheet. The duration of this interval is given by:

$$ t_f = \frac{2L_Q_{diode}}{-R_g + \frac{4L_s Q_{diode}}{Q_{gd}} (V_{dr} - V_{pl})} $$

where $Q_{diode}$ is the total capacitive charge of the junction capacitor of the fast diodes, which could be found in datasheet of the diode. It should be noted that the capacitive charge loss of the diode is counted in the MOSFET turn-on procedure but not included in this interval (though $t_f$ is related to $Q_{diode}$);

4) Gate voltage $V_g$ continues to rise, resulting in further reduction of the MOSFET drain to source on-resistance. There is no switching loss in this interval; the device is considered to be fully on after this interval.

Accordingly, the turn-on loss energy in this switching is given by:

$$ E_{on} = \frac{1}{2} V_{out} I_{load} (t_r + t_f) + \frac{1}{2} Q_{diode} V_{out}$$

where $V_{out}$ is the DC bus voltage. Different load current may lead to different turn-on energy. Thus, based on (1), (2) and (3), the relationship between $E_{on}$ and load current, namely, $E_{on}$ vs. $I_{load}$, may be determined. Together with simulation, from which the turn-on current at any turn-on instant is
modeled, the turn-on loss of MOSFETs is calculated mathematically.

Turn-off of the MOSFET is similar to turn-on process. For brevity, the expressions are not shown here.

For core loss calculation, current waveforms in boost inductors and voltage waveforms across interface inductors have been used to predict the flux density variations in corresponding components. With this information, core loss is calculated by applying the Steinmetz equation.

### D. Semiconductor Devices Selection

Switch selection, which determines switching loss and switch conduction loss, is crucial in achieving high efficiency. For diodes, 1200 V SiC Schottky diodes (candidate including: CREE C4D10120A, C4D15120A and C4D20120A) have been selected in order to eliminate reverse recovery loss. It is worth noting that diodes not only generate conduction loss but also produce switching loss due to charging and discharging of the junction capacitance. Diodes with larger current capability have higher junction capacitance that produces more switching loss. To achieve maximum efficiency, SiC diodes should be carefully selected considering their influence on both conduction loss and switching loss. For active switches, Vienna rectifiers require four-quadrant switches to block voltage and conduct current in both directions. Two MOSFETs are selected connected in a common source configuration (thus, they can be driven by the same drive) for implementation of the requisite four-quadrant switches. Several 600 V (or 650 V) Si MOSFETs (Infineon IPP60R199CP, IPW65R110CFD, IPW60R045CP) and 1200 V SiC MOSFETs (CREE C2M0160120D, C2M0080120D) have been examined in the optimization process.

### E. Inter-Phase Inductor Design and Implementation

Interleaved systems may utilize interphase inductors to mitigate circulating currents between interleaved phases, making the design an important issue in hardware implementation. However, design of the inter-phase inductor has not been explicitly described in any literature yet. Coupled inductors (like $L_{LA}$ in Fig. 2), which have high impedance seen by circulating current and very low impedance seen by non-circulating current, are selected. The impedance of the coupled inductors should be high enough so that each sub-converter can work in continuous current mode (CCM), i.e. at any fundamental half cycle, the corresponding phase current stays positive or negative. Otherwise, modulation of the converter may fail. Additionally, because circulating current flows through circuit diodes and MOSFETs, good circulating current attenuation (high coupling inductance) will not only ensure functionality but also reduce semiconductor conduction loss.

The equivalent circuit of the coupled inductor is shown in Fig. 7. From the transformer-like equivalent circuit (shown in Fig. 7(a)), a T-shape equivalent circuit (shown in Fig. 7(b)) can be easily derived, from which the inserted impedance of the inter-phase inductor is determined. In the equivalent circuit, an equivalent-parallel-capacitance (EPC), which comes from the parasitic capacitance between different layers of windings or capacitance between windings and the core of the inductor, lumped as one capacitor, is also included. At frequency range close to switching frequency, the influence of EPC can be neglected. This is always true because the total capacitance of EPC is small in general. Thus, at frequency range close to switching frequency, the relationship between circulating current peak and voltage applied across $A_1$ and $A_2$ follows:

$$I_{cr,peak} = \frac{V_{A112}}{4L_m + 2L_{th}}$$

where $I_{cr,peak}$ is the circulating current peak value, $V_{A112}$ is the voltage applied between $A_1$ and $A_2$, $t_{A112}$ is the duration of $V_{A112}$
within a certain switching period, \(L_m\) and \(L_l\) are magnetizing inductance and leakage inductance of the inter-phase inductor respectively. \(V_{A12}\) will always be half of the DC-link voltage. However, in different switching periods, \(t_{A12}\) varies a lot. To ensure that circulating current is always smaller than input current within any switching period, the basic design guideline for inductance of the inter-phase inductor in a certain switching period is:

\[
L_m > \frac{V_{A12}t_{A12}}{4I_A}
\]

where \(I_A\) is half of the total input phase current of phase A (see Fig. 2) in the certain switching period. The final value for the inductance must be greater than the largest value given by (5) when all switching periods within a fundamental period are examined. It should be noted that, different modulation schemes will result in different volt-second products being applied to the inter-phase inductor and thus different required minimum inductance values. In addition, this value only sets the lower limit for the inter-phase inductance. In real implementation, saturation and loss of the inductor should also be considered, which might result in higher inductance designs.

Another important issue in inter-phase inductor implementation is that, EPC may not be negligible at high frequencies. While the inductance of the inter-winding inductor increases the impedance of the circulating loop, EPC may have a reverse effect on the total impedance, especially at high frequency. The voltage applied to the circulating loop may contain high frequency components, e.g. drain-to-source voltage ringing when MOSFET switches (see \(V_{A1n}\) and \(V_{A2n}\) in Fig. 8, which are the voltage potentials of point \(A1\) and \(A2\) respectively, referring to middle point of DC bus). As a result, high frequency current, generated by the high frequency components of the voltage, will flow through EPC and circulate between phases (shown experimentally as \(I_{diff}\) in Fig. 8(a)), which may impede the functionality of the converter. To avoid this, the winding structure/geometry is critical. In general, bifilar winding has higher EPC than non-bifilar one. Moreover, additional coupled inductors, with superior high frequency characteristics (lower EPC), can be inserted in series with the original one to attenuate the high frequency circulating current. Circulating current with an additional high frequency coupled inductor is shown in Fig. 8(b).

**F. Converter Implementation**

Following the design procedure, we can get the relationship between boost inductance, inter-phase inductance, optimized total loss and switching frequency (shown in Fig. 9). The boost inductance needed below 22.4 kHz is determined by current harmonic limits. In the higher frequency range, power quality is no longer an issue (when...
two times of switching frequency is much higher than the highest frequency in power quality requirement, in this case, it is 32 kHz). The boost inductance is designed so that input current THD is below 10%. To achieve maximum efficiency while keeping reasonable size, switching frequency is selected to be 22.4 kHz (estimated efficiency is 99.12%).

At 22.4 kHz switching frequency, boost inductors are implemented by E55/28/21-3C90 cores with 40 turns, achieving 360 μH inductance. Inter-phase inductance is implemented by E55/28/21-3C90 cores with 40 turns, achieving 2.3 mH magnetizing inductance. Based on the loss model presented before, at 22.4 kHz switching frequency, CREE C4D15120A SiC Schottky diodes and CREE C2M0080120D SiC MOSFETs show lowest semiconductor loss, and thus, are selected.

V. EXPERIMENT RESULTS

A 3-kW converter prototype with 230 V input and 650 V output has been built (shown in Fig. 10(a)) based on the design procedure. Experimental waveforms at nominal output power are shown in Fig. 10, where $V_{\text{lin}}$ and $V_{\text{nature intro level}}$ are the voltage potentials of $A_1$ and $A_2$ (marked in Fig. 2) referred to DC bus middle point respectively. $V_{\text{lin}}$ is the voltage difference between the two voltages, which is the cause of circulating current. $I_{\text{lin}}$ and $I_{\text{nature intro level}}$ are the input currents of phase $A_1$ and phase $A_2$ (marked in Fig. 2). Their difference is shown as $I_{\text{diff}}$, which has been attenuated by the inter-phase inductor and stays close to zero. Efficiency of the converter at nominal output power measured by Yokogawa PZ4000 power analyzer is 99.08%, which matches well with the efficiency estimated by the loss calculation method described before. Additionally, with greater than 99% efficiency achieved, no active cooling is needed for this converter prototype. At nominal output power, and lab ambient, without any active cooling, case temperatures on the diodes and MOSFETs are 53 ºC and 74 ºC respectively at steady state, which is safe for the devices to work properly.

VI. CONCLUSION

This paper presents the design and hardware implementation of a three-phase interleaved Vienna converter with 99.08% efficiency. The operation principle of the interleaved Vienna rectifier is shown, with analysis on circulating current generation and attenuation. A design procedure towards optimized efficiency is proposed, where explicit loss calculations and hardware design guidelines have been presented to ensure functionality, feasibility and optimized efficiency. Finally, the experimental results validate the functionality of the proposed converter and the design procedure.

REFERENCES


